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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/678,299 | 10/06/2003 | Shunpei Yamazaki | 740756-2662 | 3512 |

22204 7590 07/18/2008

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| EXAMINER | |
|---|---|
| GEBREMARIAM, SAMUEL A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 07/18/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/678,299 | YAMAZAKI ET AL. | |
| | Examiner | Art Unit | |
| | SAMUEL A. GEBREMARIAM | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-43* is/are pending in the application.

4a) Of the above claim(s) *12-19,33 and 34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-11,20-32 and 35-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/11/08;3/27/08;5/1/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 35 and 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear how an entire top surface of the impurity region is entirely in contact with the gate insulating film as recited in claims 35 and 36. It appears from the disclosure, there are contacts formed to the impurity regions through the gate insulating film.

### *Double Patenting*

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 2, 4, 23 and 29 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 10/980,603 (603).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding claim 2, (603) teaches (claim 10) an electroluminescence display device comprising: a substrate (the EL device is inherently formed on a substrate); a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor (603, teaches a switching TFT and current-control TFT and both inherently have a gate electrode); and an electroluminescence element electrically connected to the second thin film transistor, wherein the first thin film transistor comprises at least two channel regions in an active layer (switching transistor has two TFTs and hence two channel regions), at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions (TFTs inherently have source and drain region, hence impurity regions).

The limitation of "a portable telephone" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claim 4, (603) teaches the entire claimed structure of claim 2 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (refer to claim 7).

Regarding claims 23 and 29, (603) teaches (claim 10) the entire claimed structure of claim 2 above including a display device the display device comprising a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising an active layer and at least first and second gate electrodes adjacent to the active layer with a gate insulating film interposed therebetween; a current control dement comprising a gate electrode electrically connected to the switching element; and an electroluminescence element electrically connected to the current control element.

5. Claims 5-11, 22, 24, 25-26, 28, 30 and 31-32 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 10/980,603 (603) in view of Luo, US patent No., 4,040,073.

Regarding claims 22, 24, 28 and 30, (603) teaches substantially the entire claimed structure of claims 20, 23, 27 and 29 above except explicitly stating that the wherein the substrate comprises a material selected from the group consisting of a glass, a glass ceramic, a quartz, a silicon, a ceramic, a metal, and a plastic.

Luo teaches an electroluminescence device that is based on a glass substrate (12) in order to form a device with improved stability.

It would have been have obvious to one of ordinary skill in the art at the time the invention was made to form the electroluminescence device of (603) on a glass substrate as taught by Luo in order to form a device with improved stability.

Regarding claims 5-11, 25-26 and 31-32 (603) teaches substantially the entire claimed structure of claims 2-4 above except explicitly stating that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of W2/L2> 5×W1/L1 establishes where a channel length of the second thin film transistor is L2 (0.1-50μm), a channel width of the second thin film transistor is W2 (0.5 to 30μm), a channel length of the first thin film transistor is L1 (0.2 to 18μm) and a channel width of the first thin film transistor is W1 (0.1 to 5μm).

Luo teaches a switching thin film transistor T1 and a current control TFT T2, where the channel width can be adjusted depending on the function of the device (col. 3, lines 45-55).

It would have been have obvious to one of ordinary skill in the art at the time the invention was made to adjust a channel width of the second thin film transistor and a

channel width of the first thin film transistor as claimed as taught by Luo in the structure of (603) in order to form a device with improved stability (col. 2, lines 16-25).

Furthermore parameters such as channel length and channel width in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the channel length and channel width as claimed in the structure of (603) in order to form a device with improved stability (col. 2, lines 16-25).

6. Claims 2-4, 23, 25 and 29 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of copending Application No.10/337,391 (391).

Regarding claim 2, (391) teaches (claims 1 and 5) a portable telephone comprising (claim 5, portable information terminal): an electroluminescence display device comprising: a substrate (the EL device is inherently formed on a substrate); a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor (603, teaches a switching TFT and current-control TFT and both inherently have a gate electrode); and an electroluminescence element electrically connected to the second thin film transistor, wherein the first thin film transistor comprises at least two channel regions in an active layer (switching transistor has two TFTs and hence two channel regions), at least two gate electrodes

corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions (LDD regions).

Furthermore the limitation of "a portable telephone" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claim 3, (391) teaches (claim 1) the entire claimed structure of claim 2 above including each of the first and second thin film transistors has at least one lightly doped impurity region between a channel region and at least one of a drain or the impurity region the lightly doped impurity region of the first thin film transistor does not overlap a gate electrode of the first thin film transistor and the lightly doped impurity region of the second thin film transistor overlaps a gate electrode of the second thin film transistor at least partly.

Regarding claims 4, 20, 21, 23, 27 and 29 (391) teaches the entire claimed structure of claims 2 and 3 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (refer to claim 1).

7. Claims 22, 24, 28 and 30 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of copending Application No. 10/333,391 (391) in view of Luo, US patent No., 4,040,073.

Regarding claims 22, 24, 28 and 30, (391) teaches substantially the entire claimed structure of claims 20, 23, 27 and 29 above except explicitly stating that the wherein the substrate comprises a material selected from the group consisting of a glass, a glass ceramic, a quartz, a silicon, a ceramic, a metal, and a plastic.

Luo teaches an electroluminescence device that is based on a glass substrate (12) in order to form a device with improved stability.

It would have been have obvious to one of ordinary skill in the art at the time the invention was made to form the electroluminescence device of (391) on a glass substrate as taught by Luo in order to form a device with improved stability.

Regarding claims 5-11, 25-26 and 31-32 (391) teaches substantially the entire claimed structure of claims 2-4 above except explicitly stating that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of W2/L2> 5×W1/L1 establishes where a channel length of the second thin film transistor is L2 (0.1-50μm), a channel width of the second thin film transistor is W2 (0.5 to 30μm), a channel length of the first thin film transistor is L1 (0.2 to 18μm) and a channel width of the first thin film transistor is W1 (0.1 to 5μm).

Luo teaches a switching thin film transistor T1 and a current control TFT T2, where the channel width can be adjusted depending on the function of the device (col. 3, lines 45-55).

It would have been have obvious to one of ordinary skill in the art at the time the invention was made to adjust a channel width of the second thin film transistor and a channel width of the first thin film transistor as claimed as taught by Luo in the structure of (391) in order to form a device with improved stability (col. 2, lines 16-25).

Furthermore parameters such as channel length and channel width in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the channel length and channel width as claimed in the structure of (391) in order to form a device with improved stability (col. 2, lines 16-25).

8. Claims 2-11 and 20-32 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 17-30 of copending Application No.11/258,933 (933).

Regarding claims 2-11 and 20-32, (933) teaches (claims 17-30) a portable telephone comprising (claim 22): an electroluminescence display device comprising: a substrate (the EL device is inherently formed on a substrate); a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and an electroluminescence element (pixel inherently has a display, hence electroluminescence) electrically connected to the second thin film transistor, wherein the first thin film transistor comprises at least two channel regions in an active

layer (switching transistor has two TFTs and hence two channel regions), at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions (LDD regions). Furthermore (933) teaches that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of W2/L2> 5×W1/L1 establishes where a channel length of the second thin film transistor is L2 (0.1-50μm), a channel width of the second thin film transistor is W2 (0.5 to 30μm), a channel length of the first thin film transistor is L1 (0.2 to 18μm) and a channel width of the first thin film transistor is W1 (0.1 to 5μm) (claim 3). In addition (933) teaches (claims 5-10) a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element electrically connected to the current control element, wherein each of the switching element and the current control element has at least one lightly doped impurity region where, wherein the lightly doped impurity region of the switching element does not overlap a gate electrode of the switching element and the lightly doped impurity region of the current control element overlaps a gate electrode of the current control element at least partly. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of pixels in the structure of (933), in order to form a functional display device. Furthermore (933) teaches substantially the entire claimed structure of claims 2-4 above including the substrate comprises a material selected from the group consisting of a glass, a glass

ceramic, a quartz, a silicon, a ceramic, a metal, and a plastic (refer to claim 22 and 29). Furthermore (933) teaches a portable telephone (claim 28).

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

10. Claims 2-4, 20-24 and 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Sasaki et al., US patent No. 5,790,213.

Regarding claim 2, Sasaki teaches (figs. 1-6): an electroluminescence display device comprising: a substrate (col. 8, lines 52-53, ); a plurality of pixels (col. 8, lines 37-42) over the substrate, each of the plurality of pixels comprising: a first thin film transistor (5,6); a second thin film (7) transistor comprising a gate electrode electrically connected to the first thin film transistor (fig. 2); and an electroluminescence element electrically (col. 8. lines 43-46) connected to the second thin film transistor, wherein the first thin film transistor comprises at least two channel regions in an active layer (switching transistor 5,6 has two TFTs and hence two channel regions), at least two gate electrodes corresponding to the channel regions, over the active layer with a gate

insulating film interposed therebetween, and an impurity region interposed between the channel regions (inherent device characteristics of TFT).

Furthermore the limitation of "a portable telephone" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claims 3 and 20, Sasaki teaches the entire claimed structure of claim 2 above including each of the first and second thin film transistors has at least one lightly doped impurity region between a channel region and one of a drain region or the impurity regions wherein the lightly doped impurity region of the first thin film transistor does not overlap a gate electrode of the first thin film transistor and the lightly doped impurity region of the second thin film transistor overlaps a gate electrode of the second thin film transistor at least partly (refer to fig. 2).

Regarding claims 4 and 21, Sasaki teaches the entire claimed structure of claims 2 and 20 above including the first thin film transistor (5, 6) is a switching thin film transistor and the second thin film (7) transistor is a current control thin film transistor.

Regarding claims 22-24, 27-28 and 29-30, Sasaki teaches the entire claimed structure of claims 2-4 above including the substrate is plastic glass (col. 2, line 46).

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 5-8, 9-11, 25-26 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view Luo.

Regarding claims 5, 7-8, 10-11, 25 and 31 Sasaki teaches substantially the entire claimed structure of claims 2 and 4 except explicitly stating that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of W2/L2> 5×W1/L1 establishes where a channel length of the second thin film transistor is L2 (0.1-50μm), a channel width of the second thin film transistor is W2 (0.5 to 30μm), a channel length of the first thin film transistor is L1 (0.2 to 18μm) and a channel width of the first thin film transistor is W1 (0.1 to 5μm).

Luo teaches a switching thin film transistor T1 and a current control TFT T2, where the channel width can be adjusted depending on the function of the device (col. 3, lines 45-55).

It would have been have obvious to one of ordinary skill in the art at the time the invention was made to adjust a channel width of the second thin film transistor and a

channel width of the first thin film transistor as claimed as taught by Luo in the structure of Sasaki in order to form a device with improved stability (col. 2, lines 16-25).

Furthermore parameters such as channel length and channel width in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the channel length and channel width as claimed in the structure of Sasaki in order to form a device with improved stability (col. 2, lines 16-25).

Regarding claims 6 and 9 Sasaki teaches substantially the entire claimed structure of claims 2, 4, 5 and 8 above including each of the first and second thin film transistors has at least one lightly doped impurity region between a channel region and one of a drain region or the impurity regions wherein the lightly doped impurity region of the first thin film transistor does not overlap a gate electrode of the first thin film transistor and the lightly doped impurity region of the second thin film transistor overlaps a gate electrode of the second thin film transistor at least partly (refer to fig. 2).

Regarding claims 26 and 32 Sasaki teaches substantially the entire claimed structure of claims 25 and 31 above including the substrate is glass (col. 2, line 46).

13. Claims 35, 38-39, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Ozawa et al., US 2006/0279491.

Regarding claim 35, as best the examiner is able to ascertain the claimed invention, Sasaki teaches substantially the entire claimed structure of claim 2 above except explicitly stating that wherein a top surface of the impurity region is entirely in contact with the gate insulating film.

Ozawa teaches (fig. 4) a display apparatus where wherein a top surface of the impurity region (22 and 23) is entirely in contact with the gate insulating film (50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the top surface of the impurity region that is entirely in contact with the gate insulating film as taught by Ozawa in the structure of Sasaki in order to form a display device with reduced driving voltage and improved display quality (refer to the abstract, Ozawa).

Regarding claim 38, Sasaki teaches substantially the entire claimed structure of claims 2 and 20 above except explicitly stating that in a region between the channel regions, a top surface of the active layer is entirely in contact with a gate insulating film.

Ozawa teaches (fig. 4) a region between the channel regions, a top surface of the active layer is entirely in contact with a gate insulating film.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a region between the channel regions, where a top surface of the active layer is entirely in contact with a gate insulating film as taught by Ozawa in the structure of Sasaki in order to form a display device with reduced driving voltage and improved display quality (refer to the abstract, Ozawa).

Regarding claims 39 and 41, Sasaki teaches substantially the entire claimed structure of claims 2, 23 and 27 above including in a region between the first gate electrode and the second gate electrode, a top surface of the active layer is entirely in contact with the gate insulating film (fig. 4, Ozawa).

Regarding claim 42, the combined structure of Sasaki and Ozawa teaches substantially the entire claimed structure of claims 2, 23, 27 and 29 above including each of the thin film transistors of the switching element comprises an active layer and a gate electrode with an gate insulating film therebetween, and wherein, in a region between the gate electrodes of the thin film transistors of the switching element, a top surface of the active layer is entirely in contact with the gate insulating film.

14. Claims 36, 37, 40 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Luo and in further view Ozawa et al., US 2006/0279491.

As best the examiner is able to ascertain the claimed invention, Sasaki teaches substantially the entire claimed structure of claim 5 above except explicitly stating that wherein a top surface of the impurity region is entirely in contact with the gate insulating film.

Ozawa teaches (fig. 4) a display apparatus where wherein a top surface of the impurity region (22 and 23) is entirely in contact with the gate insulating film (50).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the top surface of the impurity region that is entirely in contact with

the gate insulating film as taught by Ozawa in the structure of Sasaki in order to form a display device with reduced driving voltage and improved display quality (refer to the abstract, Ozawa).

Regarding claim 37, Sasaki teaches substantially the entire claimed structure of claim 8 above except explicitly stating that in a region between the channel regions, a top surface of the active layer is entirely in contact with a gate insulating film.

Ozawa teaches (fig. 4) a region between the channel regions, a top surface of the active layer is entirely in contact with a gate insulating film.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a region between the channel regions, where a top surface of the active layer is entirely in contact with a gate insulating film as taught by Ozawa in the structure of Sasaki in order to form a display device with reduced driving voltage and improved display quality (refer to the abstract, Ozawa).

Regarding claim 40, Sasaki teaches substantially the entire claimed structure of claim 25 above including in a region between the first gate electrode and the second gate electrode, a top surface of the active layer is entirely in contact with the gate insulating film (fig. 4, Ozawa).

Regarding claim 43, the combined structure of Sasaki and Ozawa teaches substantially the entire claimed structure of claim 31 above including each of the thin film transistors of the switching element comprises an active layer and a gate electrode with an gate insulating film therebetween, and wherein, in a region between the gate

electrodes of the thin film transistors of the switching element, a top surface of the active layer is entirely in contact with the gate insulating film.

### *Response to Arguments*

15. Applicant's arguments filed 1/4/2008 have been fully considered but they are not persuasive. Applicant argues that Sasaki discloses nothing regarding an electroluminescence element as is known to those of ordinary skill in the art. In response, it is well established in the art that most liquid crystal display devices use electroluminescence panels as backlights. Therefore the liquid crystal display inherently uses an electroluminescence element that is connected to the display device. Therefore Sasaki anticipates the claimed invention as recited above.

### *Conclusion*

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAMUEL A. GEBREMARIAM whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/SAG/
July 2, 2008